Notice of Allowability	Application No.	Applicant(s)	
	10/705,638	ROMERO ET AL.	
	Examiner	Art Unit	
	Meagan S. Walling	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/10/03 application*.

2. ☒ The allowed claim(s) is/are *1-19*.

3. ☒ The drawings filed on *10 November 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Peter Scott (Reg. 33,279) on June 8, 2005.

The application has been amended as follows:

In claims 11-18, please replace "A method of claim 1" with "A method of claim 10".

Allowable Subject Matter

Claims 1-19 are allowed.

The following is an examiner's statement of reasons for allowance:

The primary reason for the allowability of claim 1 is the inclusion of the limitation of a SCSI bus interface connector that connects the universal interface to the SCSI bus; one or more transceivers connected to the SCSI bus interface connector that convert a set of low voltage differential input signals to a set of single ended transceiver output signals; a field programmable gate array controller that receives the set of single ended transceiver output signals and provides programmed post-processing to at least a portion of the set of single ended transceiver output signals; a programmable clock connected to the field programmable gate array controller that produces a programmed clock signal that is utilized by the digital logic analyzer to synchronize data sampling on the SCSI bus; an erasable programmable read-only memory circuit connected

to the field programmable gate array controller that provides programming information for the post-processing; a set of field programmable gate array controller output signals produced by the field programmable gate array controller, the set of field programmable gate array controller output signals that in clued an output clock signal and one or more trigger signals; and an analyzer output connector that receives the set of single ended transceiver output signals and the set of field programmable gate array controller output signals and produces a digital logic analyzer input. It is this limitation in the claimed combination that has not been found taught, or suggested by the prior art of record that makes these claims allowable.

The primary reason for the allowance of claim 10 is the inclusion of the limitation of connecting to an SCSI bus with a SCSI bus interface connector on the analyzer interface board; applying power to the analyzer interface board; transferring data on the SCSI bus to one or more transceivers on the analyzer interface board that convert a set of low voltage differential signals to a set of single ended transceiver output signals; receiving and post-processing at least a portion of the set of single ended transceiver output signals with the field programmable gate array controller; applying a programmable clock signal to the field programmable gate array controller with a programmable clock to provide an output clock signal that is utilized by the digital logic analyzer to synchronize data sampling on the SCSI bus; providing programming information for the post-processing with an erasable programmable read-only memory circuit connected to the field programmable gate array; producing a set of field programmable gate array controller output signals with the field programmable gate array controller that include the output clock signal and one or more trigger signals; and receiving the set of single ended transceiver output signals and the set of field programmable gate array controller output signals

to produce a digital logic analyzer input at an analyzer output connector. It is this limitation in the claimed combination that has not been found taught, or suggested by the prior art of record that makes these claims allowable.

The primary reason for the allowance of claim 19 is the inclusion of the limitation of a SCSI bus interface connector means for connecting the universal interface to the SCSI bus; one or more transceiver means connected to the SCSI bus interface connector for converting a set of low voltage differential input signals to a set of single ended transceiver output signals; a field programmable gate array controller means for receiving the set of single ended transceiver output signals and providing programmed post-processing to at least a portion of the set of single ended transceiver output signals; a programmable clock means connected to the field programmable gate array controller means for providing a programmed clock signal that is utilized by the digital logic analyzer to synchronize data sampling on the SCSI bus; an erasable programmable read-only memory circuit means connected to the field programmable gate array controller means for providing programming information for the post-processing; a set of field programmable gate array controller output signal means produced by the field programmable gate array controller means; the set of field programmable gate array controller output signal means that include an output clock signal and one or more trigger signals; and, an analyzer output connector means for receiving receives the set of single ended transceiver output signals and the set of field programmable gate array controller output signal means for producing a digital logic analyzer input. It is this limitation in the claimed combination that has not been found taught, or suggested by the prior art of record that makes these claims allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gronlund et al. (US 5,737,520) teaches a method and apparatus for analyzing captured state logic data including memory accesses by an intelligent I/O interface device and an attached computer system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Meagan S. Walling whose telephone number is (571) 272-2283. The examiner can normally be reached on Monday through Friday 8:30 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

msw

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